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Volume Management for Fault-tolerant Continuous-flow Microfluidics

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Recent advancements in microfluidic biochips allow for easier and faster design and fabrication of increasingly complex biochips to replace conventional laboratories. A roadblock in the deployment of biochips however is their low reliability [1]. Physical defects can be introduced during the fabrication process, and may lead to failure of the biochemical application. This can be costly because of the reduced manufacturing yield, the need to redo lengthy experiments, using expensive reagents, and can be safety-critical, e.g., in case of a cancer misdiagnosis. Researchers have started to propose fault models and test techniques for continuous flow biochips [2]. Six typical defects: Block, leak, misalignment, faulty pumps, degradation of valves and dimensional errors have been identified. The resulting faults can be abstracted into blocks and leaks for simplicity [3]. Both fault types can occur in the control- as well as the flow channel, some common causes being environmental particles, imperfections in molds or bubbles in the PDMS gel. While some faults may be detected before the execution of an application by introducing a test run, other faults occur only during runtime as a result of deterioration or caused by the applied pressure. If such a fault is detected during runtime, e.g. with a CCD camera [4], we propose a just in time solution that calculates and assigns fluid volumes to alternate components and routes allowing for the completion of the application despite the occurring fault.

Fig. 1 shows a representation of an application to be executed on a biochip. Operational issues caused by faults occurring during the execution can be directly identified from this graph as well. If a leak occurs as marked in Fig. 1, we can deduce from the graph that the transport of fluid from O_2 to O_4 will be hindered and O_4 cannot be executed

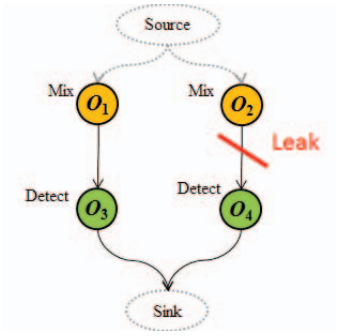

Fig. 1. Example application graph with four operations and indication of how the application is affected by the fault occurring in the architecture in Fig. 2

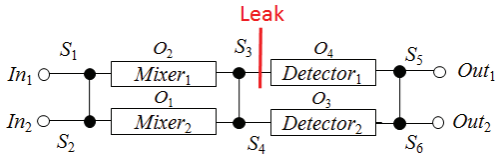

Fig. 2. Example architecture including indication of binding of operations from Fig.1 and occurring fault

successfully. Assuming a multi-purpose or fault-tolerant architecture as proposed in [1] that provides alternative routes and components through which the application can be executed, we can recalculate the volume assignment. Assuming the application from Fig. 1 is run on the architecture shown in Fig. 2, we model a leak to occur during the transport of fluid from O_2 to O_4 due to a faulty channel between S_3 and Detector_1. Since the architecture contains a second detector, the application can still be executed, using available alternative routes determined after the error . As some of the fluid is likely lost due to the occurring fault, (e.g. some fluid is lost in the leak and some is already in the no longer accessible Detector_1) new fluid assignments have to be calculated. Due to the low computational complexity of our algorithm presented in detail in [5] we can recalculate the required volumes to replenish the lost fluids during runtime and continue the execution of the application. Additionally, leftovers from the original fluid will be assigned the "Leftover Fluid" status as explained in [5], therefore allowing the fluid that was not lost in the leak to be reused and potentially reduce the volume that has to be replenished.

References

[1] P. Pop et al, *Microfluidic Very Large Scale Integration (VLSI): Modeling, Simulation, Testing, Compilation and Physical Synthesis*. Springer International Publishing, 2016.

[2] I. Araci et al, "Microfluidic very large-scale integration for biochips: Technology, testing and fault-tolerant design," in *Test Symposium (ETS), 2015 20th IEEE European*, pp. 1–8, May 2015.

[3] K. Hu, F. Yu, T. Ho, and K. Chakrabarty, "Testing of flow-based microfluidic biochips: Fault modeling, test generation, and experimental demonstration," *IEEE Transactions on Computer- Aided Design of Integrated Circuits and Systems*, vol. 33, no. 10, pp. 1463–1475, 2014.

[4] J. M. M. Alistar, P. Pop, "Redundancy optimization for error recovery in digital microfluidic biochips.," *Design Automation for Embedded Systems*, pp. 129–159, 2015.

[5] J. M. A. Schneider, P. Pop, "Waste-aware fluid volume assignment for flow-based microfluidic biochips," in *Design, Test, Integration and Packaging of MEMS and MOEMS (DTIP)*, 2017.

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